ACM8816 300W Mono, GaN HEMT Integrated, Digital Input Class-D Audio Amplifier with Rich Audio Effect Tuning

1 Features

- Flexible Power Supply Configurations
  - PVDD: 4.5V to 60V
  - DVDD and I/O: 3.3V or 1.8V
- Integrated 7mΩ R_{dson} GaN HEMT
- Excellent Efficiency and thermal performance,
  - >97% efficiency at 48V/4Ω/300W
  - Heatsink free
- Output Power capability
  - 1×160W, 4Ω, 36V, THD+N < 1%
  - 1×190W, 4Ω, 36V, THD+N < 10%
  - 1×275W, 4Ω, 48V, THD+N < 1%
  - 1×340W, 4Ω, 48V, THD+N < 10%
- Excellent Audio Performance
  - THD+N ≤ 0.03% at 1W, 1kHz, PVDD = 48V
  - 112 dB A-weighted signal-to-noise ratio (SNR)
  - Idle switching A-weighted noise ≤ 100μVrms
  - 20 mA low quiescent current
- Configurable digital audio interface
  - I^2S, Left-justified, Right-justified, TDM audio format
  - 32kHz to192kHz input sample rate
- DC Load Diagnostics
- Advanced audio effect tuning
  - Flexible digital and analog gain adjustment
  - High pass filter for DC blocking
  - Input mixer for L/R input
  - 1×15 pre BQs & 1×5 post BQs in Stereo to support enhanced audio frequency tuning
  - 3+1 band peak & RMS dynamic range control (DRC)
  - Dynamic Range Boost
  - Level Meter
- Analog protections
  - FAULT status report through GPIO and I^2C registers
  - Over current and Direct current protection
  - Over temperature protection based on external NTC and internal temperature sensor
  - Under-voltage and Over-voltage protection
  - Clock error protection

2 Applications

- Home Audio: Soundbar Woofer, HTiB (Home Theatre in a Box)
- After Market Car Audio System
- Studio Monitor
- Active Speaker
- Marine Amplifier

3 General Description

ACM8816 is a GaN HEMT integrated, high efficiency, Mono Channel Class-D audio amplifier with digital inputs. The application circuit requires few passives components to operate with 4.5V to 60V PVDD supply, 3.3V or 1.8V DVDD supply. ACM8816 integrates 7mΩ R_{dson} GaN HEMT that can drive 1×300W output power into 4Ω within 1% THD+N without heatsink required.

ACM8816 features one novel PWM modulation architecture, which adjusts PWM common duty cycle during start-up phase to avoid startup pop click.

Spread spectrum technology provides lower EMI radiated emissions. It allows inductor free application with specified output power situation with ACM8816.

The advanced audio effect tuning capability inside ACM8816 provides one highly integrated solution. It allows turning on / off each block with highly free operations. Both pre and post BQs / volume helps a lot to maintain audio headroom. Furthermore, ACME patented 3+1 band DRC with peak & RMS detection are available to implement flexible and flat multiple band control.

ACM8816 Class-H Control provides a new scheme to improve the efficiency and reduce power dissipation for battery supply system.

4 Device Information

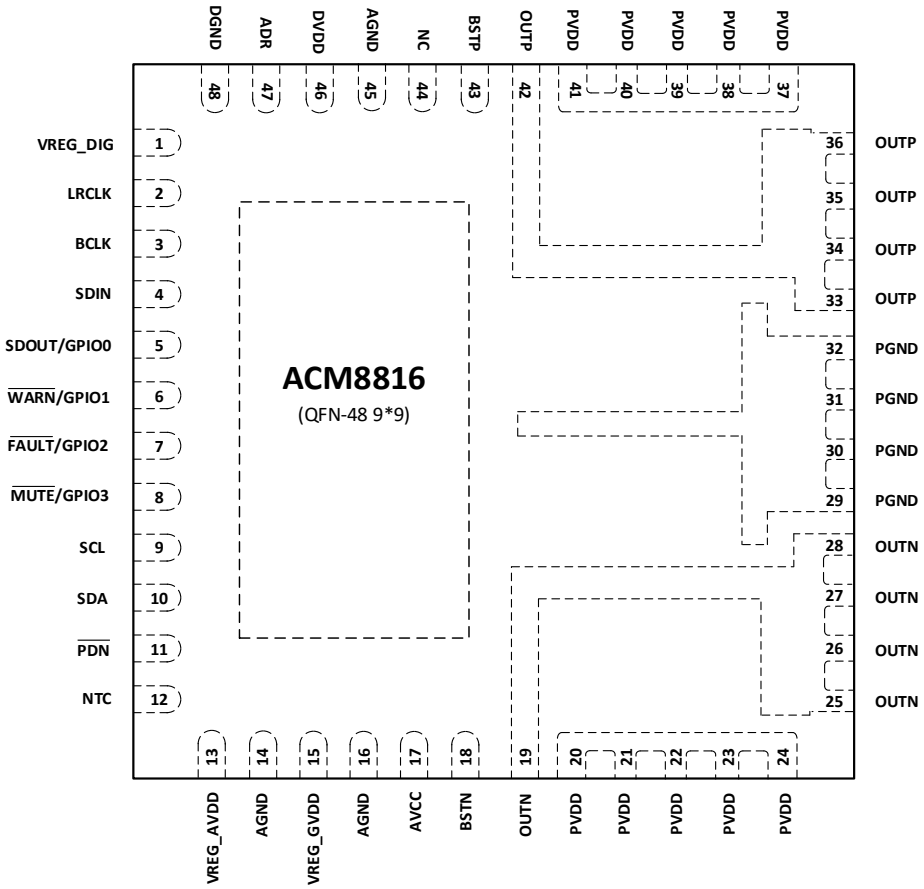
Part number	Package	Body size
ACM8816	QFN 48	9.0 mm × 9.0 mm

5 Pin Definition and Function Descriptions

ACM8816

QFN-48, 9×9mm

Top View



Pin No.	Name	Type	Description
1	VREG_DIG	AOUT	Digital regulator output.
2	LRCLK	DIN	Word select clock for the digital signal.
3	BCLK	DIN	Bit clock for the digital signal.
4	SDIN	DIN	Serial data input.
5	SDOUT / GPIO0	DIO	GPIO0: FAULT / WARNING / SDOUT…
6	WARN / GPIO1	DIO	GPIO1: FAULT / WARNING / SDOUT…
7	FAULT / GPIO2	DIO	GPIO2: FAULT / WARNING / SDOUT…
8	MUTE / GPIO3	DIO	GPIO3: FAULT / WARNING / SDOUT…
9	SCL	DIN	I^2C clock.
10	SDA	DIO	I^2C serial data.
11	PDN	DIN	Shut down, low active.
12	NTC	AIN	Temperature Sensing
13	VREG_AVDD	AOUT	Analog regulator output.
14, 16, 45	AGND	PWR	Analog ground.
15	VREG_GVDD	AOUT	Analog regulator output.
17	AVCC	PWR	Driver LDO VREG_GVDD power input. Recommend to connect to 12V.
18	BSTN	AIN	Bootstrap capacitor for OUTN.
19, 25-28	OUTN	OUT	Negative output of H-bridge.
20-24, 37-41	PVDD	PWR	Power stage supply input.
29-32	PGND	PWR	Power stage ground.
33-36, 42	OUTP	OUT	Positive output of H-bridge.
43	BSTP	AIN	Bootstrap capacitor for OUTP.
44	NC	-	Not connect.
46	DVDD	PWR	Digital power supply input: 3.3V or 1.8V.
47	ADR	DIO	I^2C address selection
48	DGND	PWR	Digital Ground.

6 Specifications

6.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
DVDD	Low-voltage digital supply	-0.3	3.9	V
AVCC	AVCC supply	-0.3	80	
PVDD	PVDD supply	-0.3	80	V
$V_{I(Digin)}$	DVDD referenced digital inputs	-0.5	V_{DVDD}+0.5	V
$V_{I(OUTxx)}$	Voltage at speaker output pins	-0.3	85	V
T_A	Ambient operating temperature	-25	85	℃
T_J	Junction Operating Temperature	-25	160	℃
T_{stg}	Storage temperature	-40	125	℃

(1) Stressed beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) DVDD referenced digital pins include: ADR, PDN, GPIO0-3, FSYNC, BCLK, SDIN, SDA, SCL.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001-2017 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002-2018 (2)	±500	

(1) JEDEC document JS-001-2017 states that 2000-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JS-002-2018 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{(SUPLLY)}$	Power supply inputs	DVDD	1.72		3.63	V
		AVCC	10.8	12	60	
		PVDD	4.5		60	
$V_{IH(DIGIN)}$	Input logic high for DVDD reference digital inputs		0.9× DVDD		DVDD	V
$V_{IL(DIGIN)}$	Input logic low for DVDD reference digital inputs				0.1×DVDD	
L_{OUT}	Minimal inductor value in LC filter under short-circuit condition		1			μH

6.4 Thermal Information

		ACM8816 QFN-48 PINS JEDEC STANDARD 4-LAYER PCB	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	TBD	℃/W
$\theta_{JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBD	℃/W
ψ_{JT}	Junction-to-top characterization parameter	TBD	℃/W

6.5 Electrical Characteristics

Free-are room temperature 25° C, BD mode, LC filter=10uH+0.47uF, Fsw=480kHz, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL I/O						
|IIH|	Input logic high current level for DVDD referenced digital input pins	$V_{IN(Digin)}=V_{DVDD}$			10	μA
|IIL|	Input logic low current level for DVDD referenced digital input pins	$V_{IN(Digin)}$=0 V			-10	μA
$V_{IH(Digin)}$	Input logic high threshold for DVDD referenced digital inputs		70%			V_{DVDD}
$V_{IL(Digin)}$	Input logic low threshold for DVDD referenced digital inputs				30%	V_{DVDD}
$V_{OH(Digin)}$	Output logic high threshold for DVDD referenced digital inputs	I_{OH} = 2mA	80%			V_{DVDD}
$V_{OL(Digin)}$	Output logic low threshold for DVDD referenced digital inputs	I_{OH} = -2mA			20%	V_{DVDD}
I²C CONTROL PORT						
$C_{L(I2C)}$	Allowable load capacitance for each I²C line				400	pF
$F_{SCL(fast)}$	Support SCL frequency	No wait states, fast mode			400	kHz
$F_{SCL(slow)}$	Support SCL frequency	No wait states, fast mode			100	kHz
SERIAL AUDIO PORT						
t_{DLY}	Required FSYNC to BCLK rising edge delay		5			ns
D_{SCLK}	Allowable SCLK duty cycle		40%		60%	
f_S	Supported input sample rates		32		192	kHz
F_{BCLK}	Supported BCLK frequencies		32		64	f_S
AMPLIFIER OPERATING MODE AND DC PARAMETERS						
t_{OFF}	Turn-off Time	Excluding volume ramp			10	ms
$A_{V(SPK\_AMP)}$	Programmable Gain	Value represents the 'peak voltage' disregarding clipping due to lower PVDD Measured at 0dB input (1FS)	11.3		67	V_{peak}/FS
$\Delta A_{V(SPK\_AMP)}$	Amplifier gain error	Gain=67 V_{Peak}/FS		0.5		dB
F_{SW}	Switching frequency of the speaker amplifier	Configured by Register Page0, reg 0x01, bit3:1		384		kHz
				480		kHz
				576		kHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
				768		kHz
				1024		kHz
				1536		kHz
				2048		kHz
$R_{DS(ON)}$	Drain-to-source on resistance of the individual output HEMTs	FET + Metallization. V_{PVDD}=48V, $I_{(OUT)}$=500mA, T_J=25℃		7		mΩ
PROTECTION						
OCE_{THRES}	Over-Current Error Threshold	Configured by Register		18		A
$UVE_{THRES(PVDD)}$	PVDD under voltage error threshold	Configured by Register		10.8		V
$UVE_{HYS(PVDD)}$	PVDD under voltage error hysteresis			0.7		V
$UVE_{THRES(AVCC)}$	AVCC under voltage error threshold			4.0		V
$UVE_{HYS(AVCC)}$	AVCC under voltage error hysteresis			0.2		V
$OVE_{THRES(PVDD)}$	PVDD over voltage error threshold			75		V
$OVE_{HYS(PVDD)}$	PVDD over voltage error hysteresis			3.5		V
DCE_{THRES}	Output DC Error protection threshold	Class D Amplifier's output DC voltage cross speaker load to trigger Output DC Fault protection		2		V
T_{DCDET}	Output DC Detect time	Class D Amplifier's output remain at or above DCE_{THRES}		620		ms
OTW_NTC_{THRES}	Over temperature protection threshold on NTC pin.	OTW Level 0		1.2		V
OTW_NTC_{HYS}	Over temperature protection hysteresis on NTC pin.			0.2		V
$OTSD\_NTC_{THRES}$	Over temperature protection threshold on NTC pin.	Over temperature shutdown threshold.		1.2		V
$OTSD\_NTC_{HYS}$	Over temperature protection hysteresis on NTC pin.			0.2		V
OTE_{THRES}	Internal Over temperature error threshold			160		℃
OTE_{HYS}	Over temperature error hysteresis			10		℃
OTW_{THRES}	Over temperature warning level			135		℃
AUDIO PERFORMANCE						
$\|V_{OS}\|$	Amplifier offset voltage	Measure differentially with zero input data, programmable gain configured with 67Vp/FS, V_{PVDD}=48V	-10		10	mV
$P_{O(SPK)}$	Output Power (Per Channel)	V_{PVDD}=36V,R_{SPK}=4Ω,f=1kHz,THD+N=10 %		190		W
		V_{PVDD}=36V,R_{SPK}=4Ω,f=1kHz,THD+N=1%		160		W
		V_{PVDD}=48V,R_{SPK}=4Ω,f=1kHz,THD+N=10 %		340		W
		V_{PVDD}=48V,R_{SPK}=4Ω,f=1kHz,THD+N=1%		275		W

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$THD+N_{SPK}$	Total harmonic distortion and noise (P_O=1W,f=1kHz,R_{SPK}=4Ω)	V_{PVDD}=36V		0.03		%
		V_{PVDD}=48V		0.03		%
$ICN_{(SPK)}$	Idle channel noise (A-Weighted, AES17)	V_{PVDD}=48V, LC filter=10uH+0.47uF, Load=4Ω		100		μVrms
DR	Dynamic range	A-Weighted, -60dBFS method. V_{PVDD}=48V， Analog Gain=67Vp/FS		110		dB
SNR	Signal-to-noise ratio	A-Weighted, reference to 1% THD+N Output Level, V_{PVDD}=48V		112		dB
PSRR	Power supply rejection ratio	Injected Noise=1kHz, 1Vrms, V_{PVDD}=24V, input audio signal=digital zero		72		dB

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
Serial Audio Port Timing-Slave Mode					
f_{BCLK}	BCLK frequency	1.024			MHz
t_{BCLK}	BCLK period	40			ns
t_{BCLKL}	BCLK pulse width, low	16			ns
t_{BCLKH}	BCLK pulse width, high	16			ns
t_{BF}	BCLK rising to FSYNC edge	8			ns
t_{FB}	FSYNC Edge to BCLK rising edt	8			ns
t_{SU}	Data setup time, before BCLK rising edge	8			ns
t_{DH}	Data hold time, after BCLK rising edgeD	8			ns
t_{DFB}	Data delay time from BCLK failing edge		30		ns
I^2C Bus Timing-Standard					
f_{SCL}	SCL clock frequency			100	kHz
t_{BUF}	Bus free time between a STOP and START condition	4.7			μs
t_{LOW}	Low period of the SCL clock	4.7			μs
t_{HI}	High period of the SCL clock	4			μs
t_{RS-SU}	Setup time for (repeated) START condition	4.7			μs
t_{S-HD}	Hold time for (repeated) START condition	4			μs
t_{D-SU}	Data setup time	250			ns
t_{D-HD}	Data hold time	0		3450	ns
t_{SCL-R}	Rise time of SCL signal			1000	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit			1000	ns
t_{SCL-F}	Fall time of SCL signal			1000	ns
t_{SDA-R}	Rise time of SDA signal			1000	ns
t_{SDA-F}	Fall time of SDA signal			1000	ns
t_{P-SU}	Setup time for STOP condition	4			μs
C_B	Capacitive load for each bus line			400	pf
I^2C Bus Timing-Fast					
f_{SCL}	SCL clock frequency			400	kHz
t_{BUF}	Bus free time between a STOP and START condition	1.3			μs
t_{LOW}	Low period of the SCL clock	1.3			μs

		MIN	NOM	MAX	UNIT
t_{HI}	High period of the SCL clock	600			ns
t_{RS-SU}	Setup time for (repeated) START condition	600			ns
t_{RS-HD}	Hold time for (repeated) START condition	600			ns
t_{D-SU}	Data setup time	100			ns
t_{D-HD}	Data hold time	0		900	ns
t_{SCL-R}	Rise time of SCL signal	$20+0.1C_B$		300	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20+0.1C_B$		300	ns
t_{SCL-F}	Fall time of SCL signal	$20+0.1C_B$		300	ns
t_{SDA-R}	Rise time of SDA signal	$20+0.1C_B$		300	ns
t_{SDA-F}	Fall time of SDA signal	$20+0.1C_B$		300	ns
t_{P-SU}	Setup time for STOP condition	600			ns
t_{SP}	Pulse width of spike suppressed			50	ns
C_B	Capacitive load for each bus line			400	pf

6.7 Timing Parametric Requirements Information

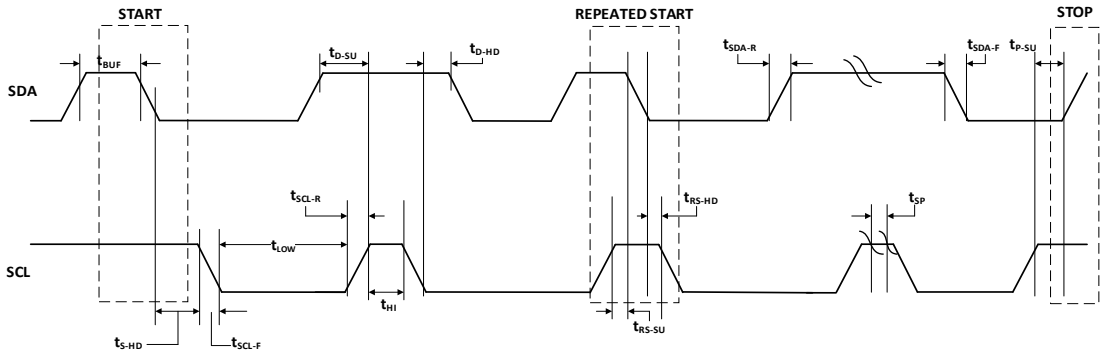


Figure 1 I²C Communication Port Timing Diagram

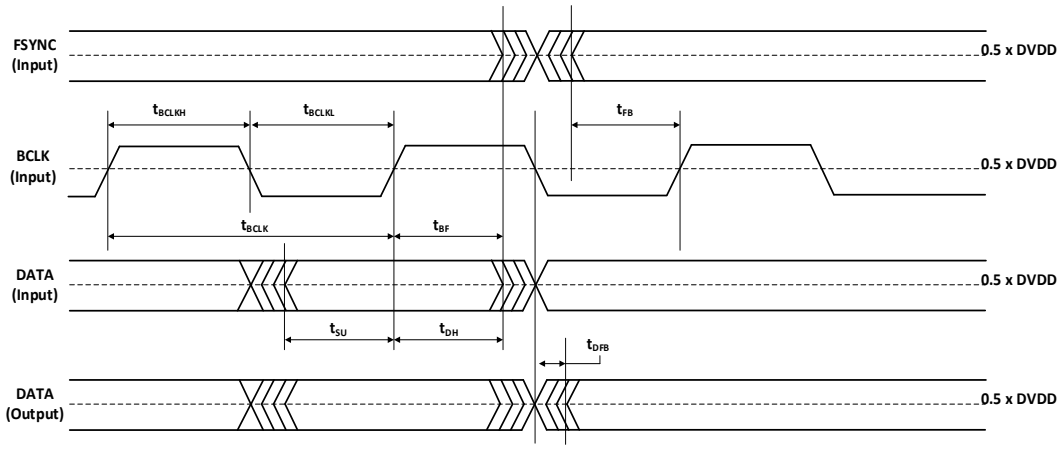
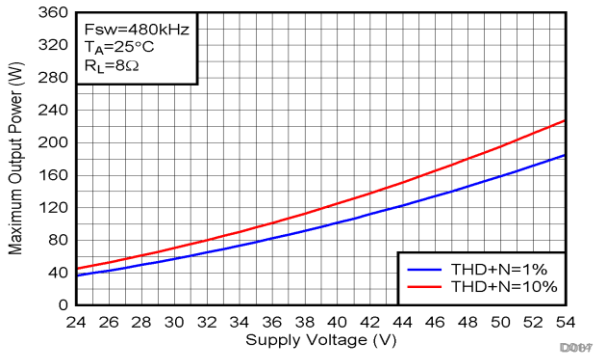


Figure 2 Serial Audio Port Timing in Slave Mode

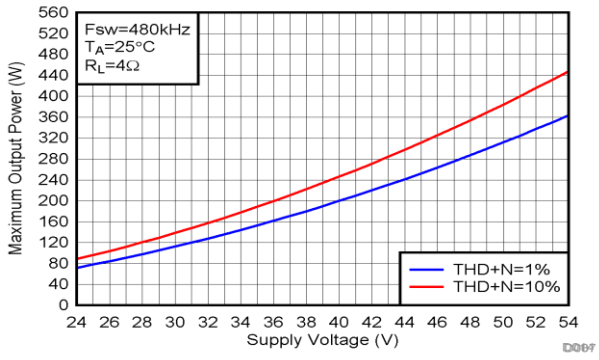
7 Typical Characteristics

Free-air room temperature 25℃ (unless otherwise noted). ACM8816 EVM board, device PWM Modulation mode set to High Performance mode with 480kHz Fsw.



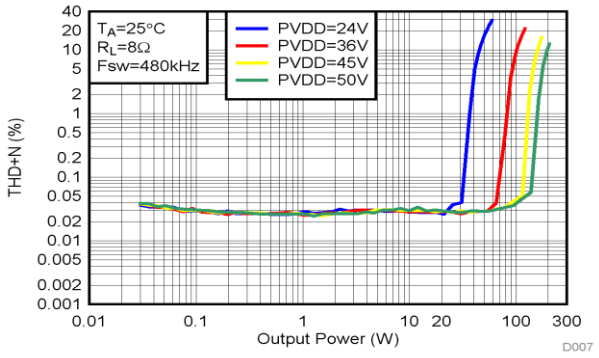
(Load=8Ω, Fsw=480kHz)

Figure 1 Output Power vs PVDD



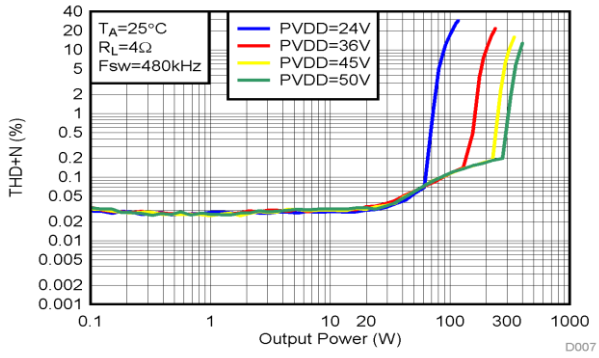
(Load=4Ω, Fsw=320kHz)

Figure 2 Output Power vs PVDD



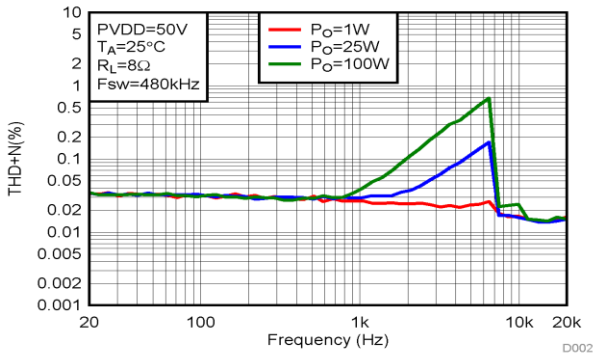
(Load=8Ω, Fsw=480kHz)

Figure 5 THD+N vs Output Power



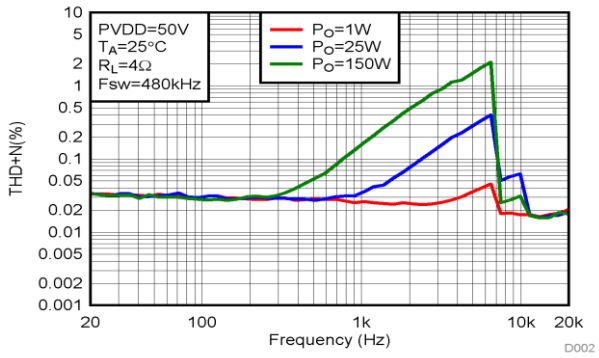
(Load=4Ω, Fsw=480kHz)

Figure 6 THD+N vs Output Power



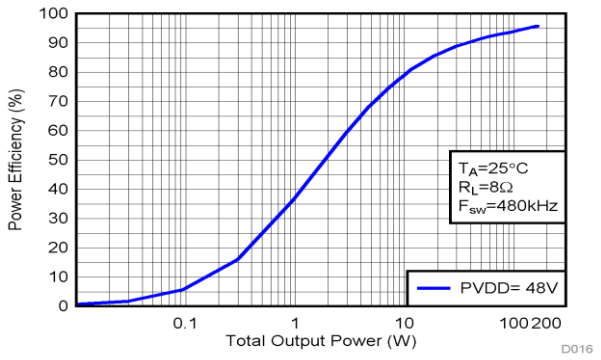
(Load=4Ω, PVDD=50V, Fsw=480kHz)

Figure 9 THD+N vs Frequency



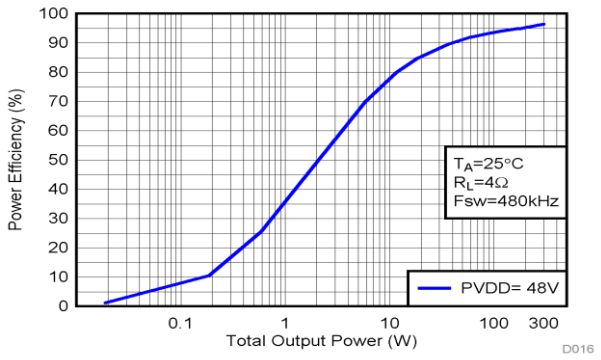
(Load=8Ω, PVDD=50V, Fsw=480kHz)

Figure 10 THD+N vs Frequency



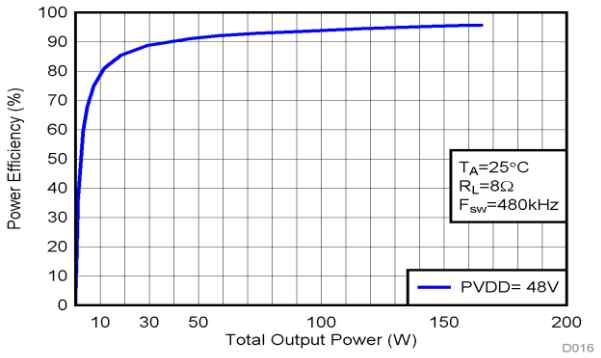
(Load=8Ω, Fsw=480kHz, PVDD=48V)

Figure 13 Efficiency (Log scale)



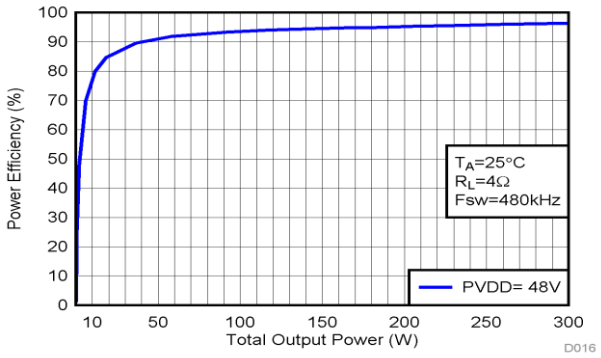
(Load=4Ω, Fsw=480kHz, PVDD=48V)

Figure 14 Efficiency (Log scale)



(Load=8Ω, Fsw=480kHz, PVDD=48V)

Figure 13 Efficiency



(Load=4Ω, Fsw=480kHz, PVDD=48V)

Figure 14 Efficiency

8 Detailed Description

8.1 Overview

The ACM8816 device integrates 5 main building blocks together into a single cohesive device that maximizes sound quality, flexibility, and ease of use. The 5 main building blocks are listed as follows:

- An audio DAC
- An audio effect tuning block
- A flexible closed-loop amplifier, at different switching frequencies, and supporting a variety of output voltages and loads
- An I^2C control port for communication with the device
- Power stage consists of low R_{dson} GaN HEMT

The device requires three power supplies for proper operation. A DVDD supply is required to power the internal LDO and generate VREG_DVDD for internal low voltage digital circuitry. AVCC is required to provide the power supply for internal analog circuitry, including two internal LDOs to output 5V for VREG_AVDD and for VREG_GVDD respectively. Another supply, called PVDD, is required to provide power to the output stage of the audio amplifier.

8.2 Functional Block Diagram

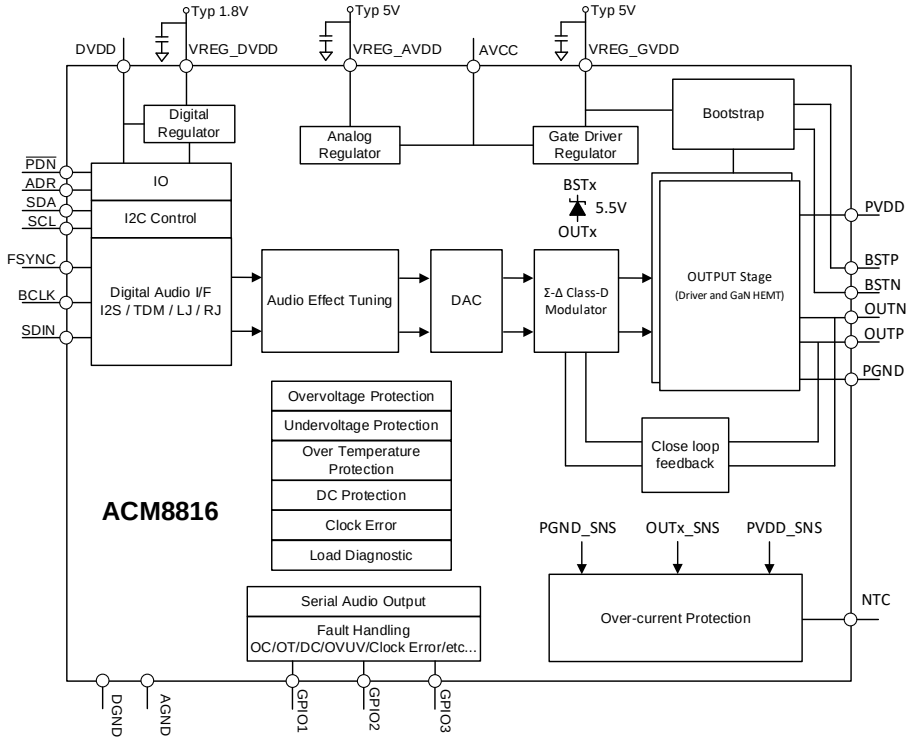


Figure 17 Function Block Diagram

8.3 Device Clocking

8.3.1 Main Clocks

The ACM8816 device has flexible systems for clocking. Internally, the device requires a number of clocks, mostly at related clock rates to function correctly. All of these clocks can be derived from the Serial Audio Interface.

The serial audio interface typically has 3 connection pins which are listed as follows,

- BCLK
- FSYNC/LRCLK (Left/Right Word Clock and Frame Sync)
- SDIN (Input Data)

The device has an internal PLL that is used to take BCLK as reference clock and create the higher rate clocks required by the Audio Effect Tuning and the DAC clock.

The ACM8816 device has an audio sampling rate detection circuit that automatically senses the sampling frequency. Common audio sampling frequencies of 32kHz, 44.1kHz-48kHz, 88.2kHz-96kHz, 176.2kHz-192kHz are supported. The sampling frequency detector sets the clock for DAC and Audio Effect Tuning automatically.

8.3.2 Serial Audio Port – Clock Rates

The serial audio interface port is a 3-wire serial port with the signals FSYNC/LRCLK, BCLK, and SDIN. BCLK is the serial audio bit clock, used to clock the serial data present on SDIN into the serial shift register of the audio interface. Serial data is clocked into the ACM8816 device on the rising edge of BCLK. The FSYNC/LRCLK pin is the serial audio left/right word clock or frame sync when the device is operated in TDM mode.

Table 1. Audio Data Formats, Bit Depths and Clock Rates

FORMAT	DATA BITS	MAXIMUM LRCLK/FS FREQUENCY (kHz)	BCLK RATE (Fs)
I²S/LJ/RJ	32,24,20,16	32 to 96	64,32
TDM	32,24,20,16	32	128
		44.1/48	128,256,512
		88.2/96	128,256
	32,24,20,16	176.4/192	128

When clock halt, non-supported BCLK to FSYNC/LRCLK ratio is detected, the device reports clock error in Register 0x18 on Page0.

8.3.3 Clock Halt Auto-recovery

As some of host processor Halts I²S clock when there is no audio playing. After clock halt, the device puts all channels into Hi-Z state and reports clock error in register 0x18 on Page0. After audio clock recovery, the device automatically returns to the previous state.

8.3.4 Sample Rate on The Fly Change

ACM8816 supports FSYNC/LRCLK rate on the fly change. For example, change FSYNC/LRCLK from 32kHz - 192kHz, Host processor needs to put LRCLK (FSYNC) to Halt state at least 10ms before changing to new sample rate.

8.3.5 Serial Audio Port – Data Formats and Bit Depths

The device supports industry-standard audio data formats, including standard I²S, left-justified, right-justified and TDM/DSP data. Data formats are selected via Register Page0/0x07. If the high width of FSYNC/LRCLK in TDM/DSP mode is less than 8 cycles of BCLK, the register Page0/0x07 D[5:4] should be set to 01. All formats require binary two's complement, MSB-first audio data, up to 32-bit audio data is accepted. All the data formats, word length and clock rate supported by this device are shown in Table 1. The data formats are detailed in Figures below. The word length is selected via Register Page0/0x07 D[1:0]. The offset of data is selected via Register Page0/0x08.

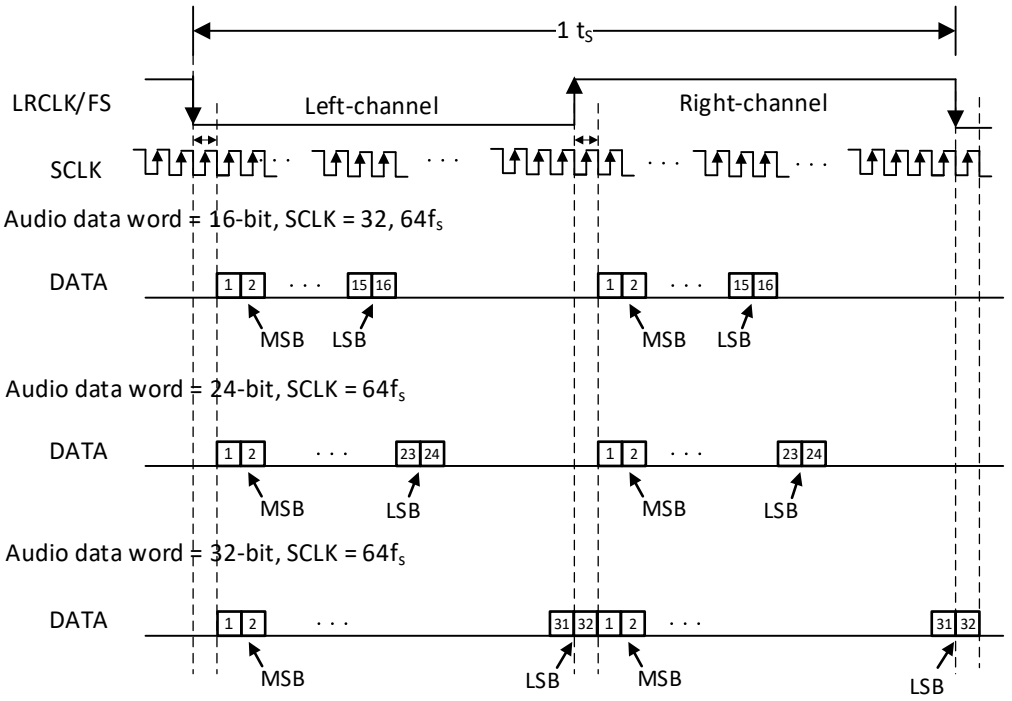


Figure 18 I²S Audio Data Format

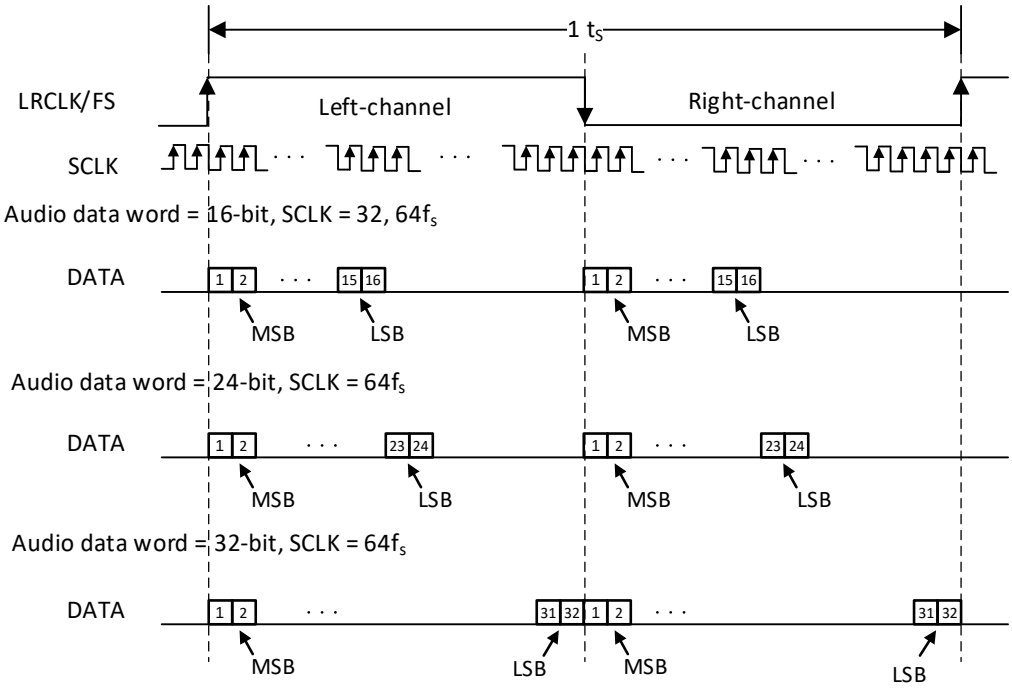
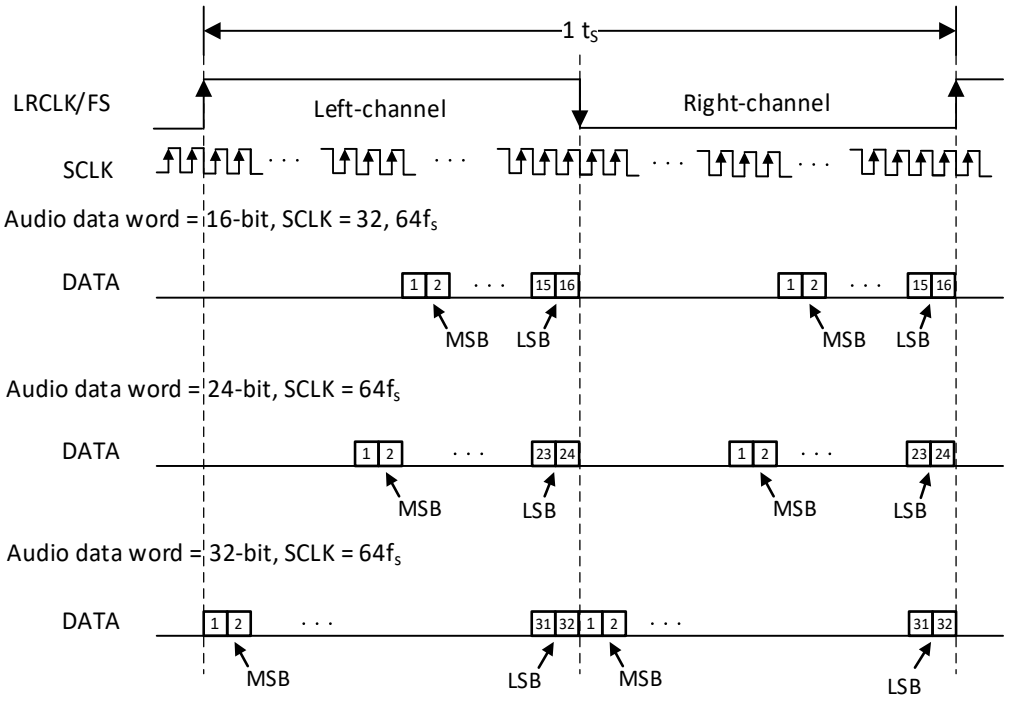
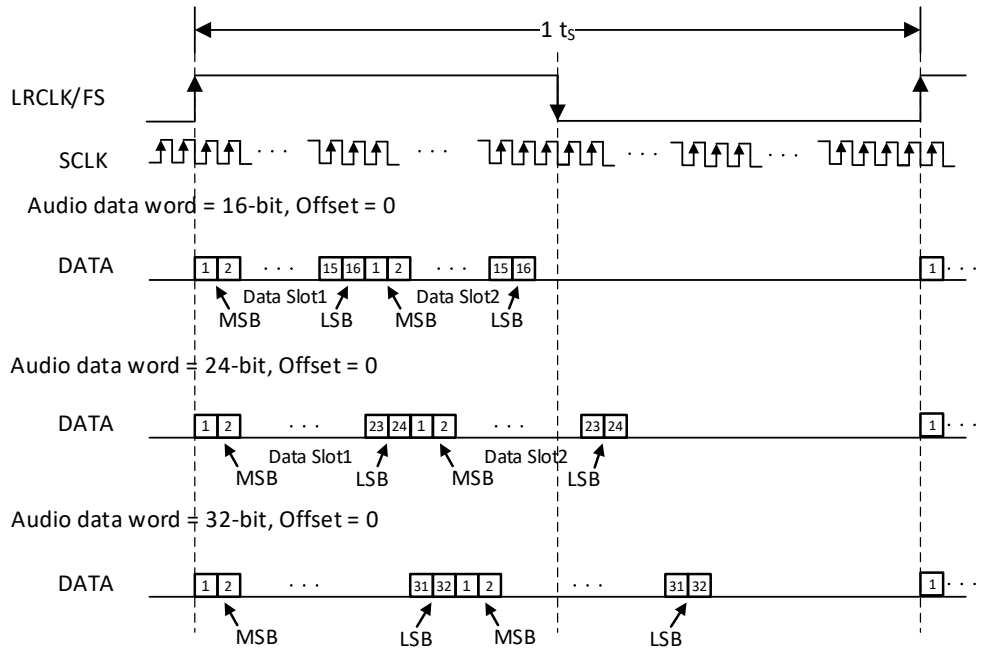


Figure 19 Left-Justified Audio Data Format



Right-Justified Data Format; L-channel = HIGH, R-channel = LOW

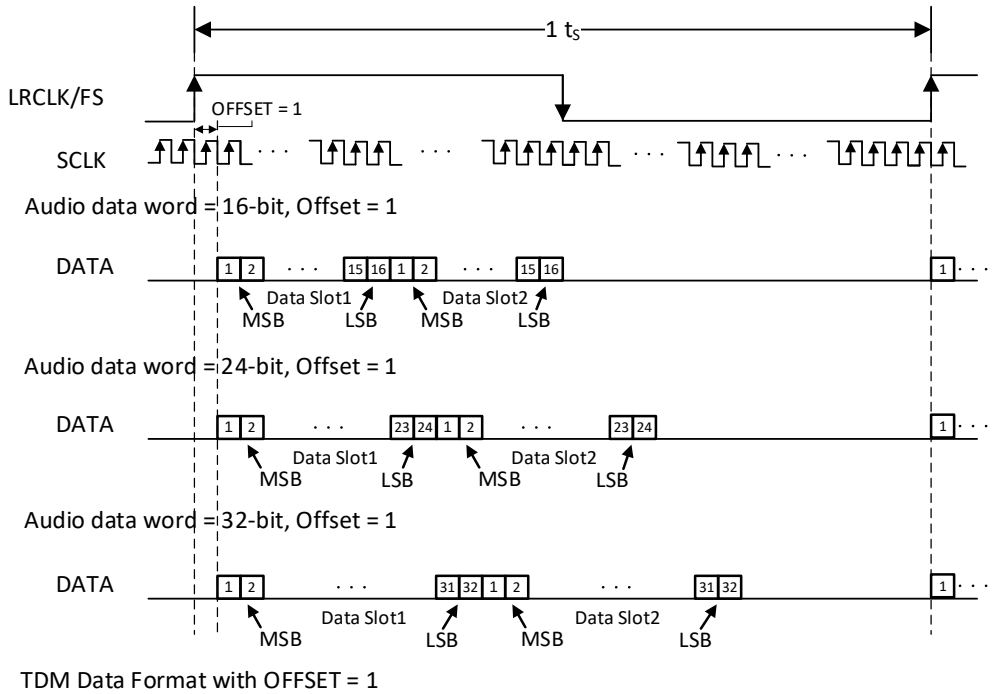
Figure 20 Right-Justified Audio Data Format



TDM Data Format with OFFSET = 0

In TDM Modes, Duty Cycle of LRCLK/FS should be 1× SCLK at minimum. Rising edge is considered frame start

Figure 21 TDM 1 Audio Data Format



In TDM Modes, Duty Cycle of LRCLK/FS should be 1× SCLK at minimum. Rising edge is considered frame start

Figure 22 TDM 2 Audio Data Format

8.4 Power Supplies

To facilitate system design, ACM8816 needs three external power supplies.

DVDD, a 3.3-V or 1.8-V supply for internal DVDD_REG LDO to generate a 1.8V rail on VREG_DIG pin to power the internal digital circuitry.

AVCC, a 12-V(in nominal) supply to power the two internal voltage regulators AVDD/GVDD to provide suitable voltage levels for the gate driver circuitry and other internal analog circuitry. The external pins are provided only as a connection point for off-chip bypass capacitors for decoupling. Connecting external circuitry to these regulators may result in reduced performance and damage to the device. The AVCC has the same voltage tolerance capability with PVDD, which is up to 60V. However, as the AVDD/GVDD LDO is 5V output, thus a supply voltage of 12V is recommended to for the AVCC to avoid the unnecessary power dissipation.

PVDD, supply for the GaN HEMT power stage.

8.5 Gate Driver and GaN HEMTs

The gate driver accepts the low-voltage PWM signal and level shifts it to drive a high current H-bridge stage formed by GaN HEMTs. The gate driver is powered by GVDD, which is generated by internal LDO. The decoupling capacitor for GVDD must be placed as close as possible to the VREG_GVDD pin.

The power stage is formed by 4 GaN HEMTs as an H-bridge. Therefore, bootstrap capacitors are required for the normal operation of the high side GaN HEMTs. A 0.47μF ceramic capacitor with 16V and X7R rated or better, is recommended. The bootstrap capacitors should be connected across the OUTx pin and the corresponding BSTx pin. The bootstrap capacitors function as the floating power supply for the high-side GaN HEMTs gate drive circuitry. During each high side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high to maintain the high side HEMTs turned on.

The ACM8816 employs integrated ultra-low $R_{ds(on)}$ GaN HEMTs, which is typically 7mΩ, to achieve high efficiency, excellent thermal and maximize the output power from a given power supply voltage rail. These GaN HEMTs are designed to run in high switching frequency and could withstand as high as 80V voltage transients during load dump event.

8.6 Device Gain Setting

As seen in the figure below, the audio path of the ACM8816 consists of a digital audio input port, a digital audio path, a digital to PWM convertor, a gate driver stage, a Class D power stage, and the feedback loop which feeds the output information back into the digital to PWM block to correct for distortion sensed on the output pins. The total amplifier gain is comprised of digital gain in the digital audio path and the analog gain from the input of the analog modulator to the output of the speaker amplifier power stage.

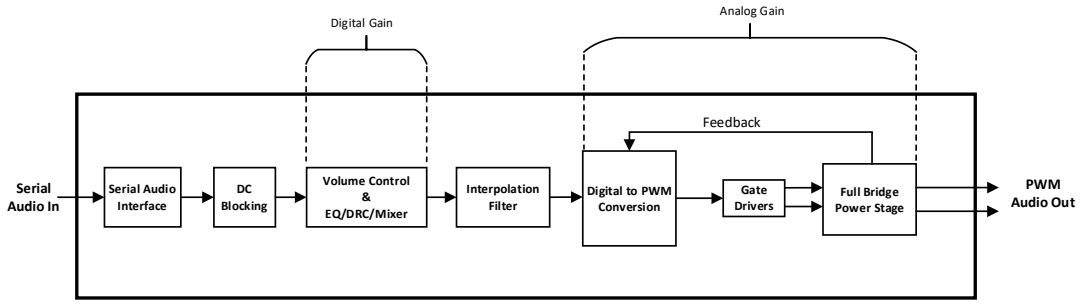


Figure 23. Gain Structure

As shown above, the first gain stage for the speaker amplifier is present in the digital audio path. It consists of the volume control and EQ/DRC/Mixer. The volume control is set to 0dB by default and EQ/DRC/Mixer is bypassed by default.

Amplifier analog gain settings are presented as the output level in dBV (dB related to 1Vrms) with a full-scale serial audio input (0dBFS) and the digital volume control set to 0dB.

V_{AMP}=Input +Digital Gain + Analog Gain dBV

Where:

- V_{AMP} is the amplifier output voltage in dBV_{RMS}
- Input is the digital input amplitude in dB with respect to 0dBFS
- Digital Gain is the digital volume control setting, -110dB to 24dB.
- Analog Gain is the analog gain setting (33.5dBV_{rms} to 18.0dBV_{rms} in 0.5dB per step)

Table 2 outlines gain setting expressed in dBV_{RMS} and V_{PEAK}.

Table 2 Amplifier Gain Settings

Analog Gain	**FULL SCALE OUTPUT**	
(Register 0x02h in Page0)	**dBV_{RMS}**	**V_{PEAK}**
00000	33.5	67
00001	33.0	63.25
00010	32.5	59.71
00011	32.0	56.37
…	…	…
01110	26.5	29.92
01111	26.0	28.25

10000	25.5	26.67
…	…	…
11111	18.0	11.25

8.7 Device Protection and Status Monitoring

8.7.1 Cycle-by-cycle Current Limit

The Cycle-by-Cycle (CBC) current limit terminates each PWM pulse to limit the output current when the user defined CBC level in Page0/0x21 D[7:5]is reached. With this feature, the output power is limited but the music playing continues without disruption and prevents undesired over current shutdown during audio peaks. Each channel is monitored and limited independently.

Depending on the CBC active duration, the device takes no action, or report as warning to register and WARN pin.

8.7.2 Over Current Protection

If the output current exceeds the over current shutdown threshold, I_{OCP}, such as the any of the output suddenly short to GND or power supply, an over current shutdown (OCSD) event is triggered. Each channel current is monitored, limited, and reported independently. Once an OCSD event is triggered, the device shuts down the affected channel and transfer its state to Sleep.

By default, the OCSD event is reported as fault to register and FAULT pin.

To recover from fault condition and back to normal operation, the user needs to write to Page0/0x01 D[7] to clear the fault.

8.7.3 DC Detection

The ACM8816 monitors the DC offset continuously during normal operation at the output. If any channel's DC output exceeds the DC_{DETECT} threshold, the channel triggers a DC Fault Event and is transferred to Sleep state.

By default, the DC event is reported as fault to register and FAULT pin.

8.7.4 Clip Detection

The ACM8816 monitors the output signal for voltage clipping situation. Each channel is monitored and reported independently. The clip level to create a clip event could be configured in the DSP registers.

By default, the Clip event is reported as warning to register and WARN pin.

8.7.5 Over-temperature Warning and Shutdown

The ACM8816 integrates an on-chip temperature sensor that used to monitor the junction temperature of the device. Besides, the ACM8816 has an NTC input pin, that can be used to monitor the local temperature where the heat is mostly concentrated on the PCB. The OTW and OTSD threshold in NTC voltage is shown as the table below,

Table 3. OTW/OTSD Threshold in NTC voltage

	OTW0 (NTC)	OTW1 (NTC)	OTSD (NTC)
Threshold	1.1V	1.2V	1.68V
Hysteresis	0.2V	0.2V	0.28V

The OTW0 and OTW1 selection locates on Page0/0x20 D[5].

8.7.6 PVDD/GVDD and Temperature Sense

The ACM8816 integrates SAR ADCs to sense and report the real-time PVDD supply voltage, GVDD voltage, NTC pin Voltage and die temperature. The conversions are active in HiZ and Play state.

The PVDD voltage result is available in Page0/0x32 D[7:0], with the conversion equation as below,

$$PVDD\ Voltage\ (V) = 85 * code\ in\ DEC\ /255$$

The GVDD voltage result is available in Page0/0x34 D[7:0], with the conversion equation as below,

$$GVDD\ Voltage\ (V) = 8 * code\ in\ DEC\ /255$$

The NTC voltage result is available in Page0/0x35 D[7:0], with the conversion equation as below,

$$NTC\ Voltage\ (V) = 2.5 * code\ in\ DEC\ /255$$

The die temperature result is available in Page0/0x33 D[7:0], with the conversion equation as below,

$$Die\ Temperature(℃) = -57 + code\ in\ DEC$$

8.7.7 Overvoltage and Load-dump

When PVDD supply voltage rises above the $OVE_{THRES(PVDD)}$, the over voltage protection is triggered and the device enters Sleep state. When the PVDD supply voltage falls to the voltage lower than ($OVE_{THRES(PVDD)}$ - $OVE_{HYS(PVDD)}$), the device recovers normal operation automatically. The register fault flag and the pulled-low fault pin are not latched, which means they would automatically recover until the fault condition is removed.

By default, the over voltage event is reported as fault to register and FAULT pin. The device can withstand 80 V load dump voltage surges.

8.7.8 Undervoltage and Power-on-reset

When PVDD supply voltage falls below the $UVE_{THRES(PVDD)}$, or the AVCC supply voltage falls below the $UVE_{THRES(AVCC)}$, the undervoltage protection is triggered and the device enters Sleep state. When the PVDD supply voltage rises to the voltage higher than ($UVE_{THRES(PVDD)}$ + $UVE_{HYS(PVDD)}$) and AVCC supply voltage rises to the voltage higher than ($UVE_{THRES(AVCC)}$ + $UVE_{HYS(AVCC)}$), the device recovers normal operation automatically. The register fault flag and the pulled-low fault pin are not latched, which means they would automatically recover until the fault condition is removed.

By default, the undervoltage event is reported as fault to register and FAULT pin.

8.7.9 Clock Fault

In HiZ and Play mode, the ACM8816 monitors the audio serial interface for clock fault detection. Once a clock fault event is triggered when in play mode, the device enters HiZ state. The device recovers normal operation automatically when the fault condition is removed. The register fault flag and the pulled-low fault pin would not recover until the fault is cleared manually by writing to Page0/0x01 D[7].

By default, the clock fault event is reported as fault to register and FAULT pin.

8.8 Class H Control

ACM8816 Class-H Control provides a new scheme to increase efficiency and reduce power dissipation for battery supply system. ACM8816 internal Class H block monitors the digital audio signal and provides control signal to

feedback network of external DC-DC Boost Convertor, adjust Boost Convertor's V_{OUT} accordingly. As ACM8816 use the external Booster Convertor's V_{OUT} as the power supply, so ACM8816's Power supply dynamic tracking with output audio signal, shown in Figure below.

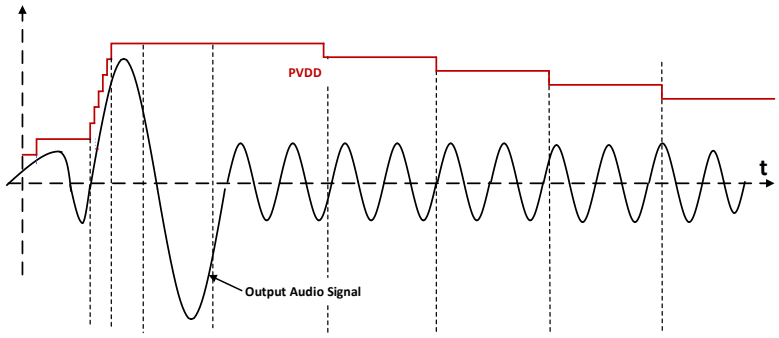
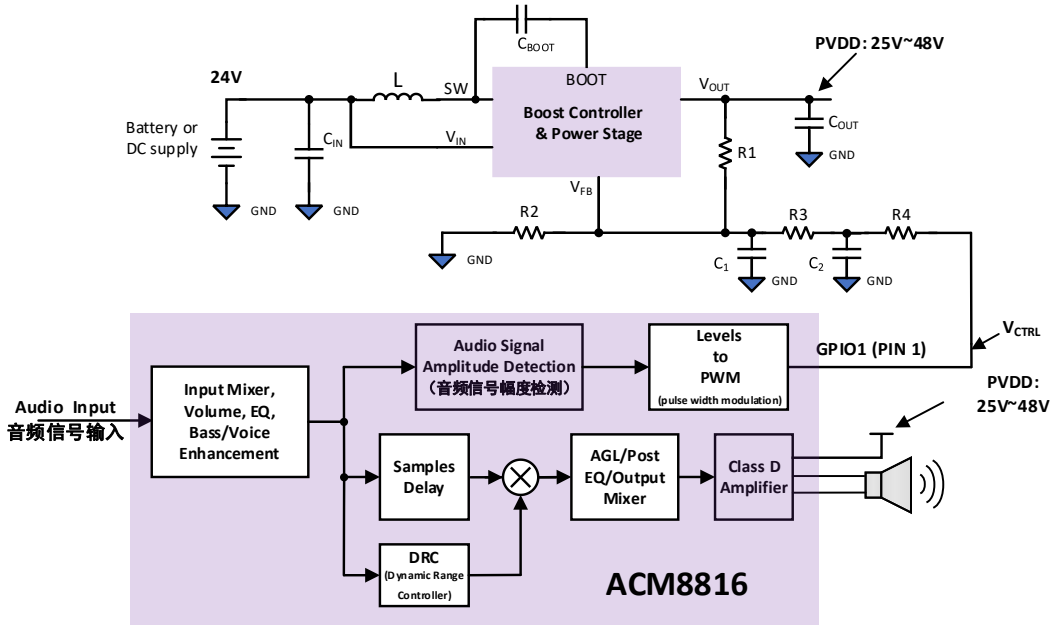


Figure 24. Class H Operation Signal

ACM8816 employs an internal Audio Signal Amplitude Detection Block for audio signal amplitude detection, as the target PVDD range and the amplifier system gain is known, so the digital input levels in 'Levels to PWM' block will calculate the proper digital input levels and transfers to different duty cycle. Generally, ACM8816 supports 16 levels Class H Control. For example, if the PVDD range is 25V-48V, the PVDD tracking with output audio signals by following values: { 25V, 26.5V, 28.1V, 29.6V, 31.1V, 32.6V, 34.2V, 35.7V, 37.3V, 38.8V, 40.3V, 41.8V, 43.4V, 45V, 46.5V, 48V }. Based on detailed system application requirement (PVDD min/max value, V_{FB} of the Booster Convertor, DVDD value, R2), ACME Audio Tuning software generates corresponding register configuration and external BOM which shown in Figure below.



$$\frac{V_{OUT}-V_{FB}}{R1} = \frac{V_{FB}}{R2} + \frac{V_{FB}-V_{CTRL}}{R3+R4}$$

Figure 25. Class H Control Block

8.9 Spread Spectrum

Spread Spectrum distributes the narrowband PWM switching signal into a wideband signal, which spreads the energy across a specific frequency range. The ACM8816 offers several spread spectrum options to improve the EMC

performance, including various spread-spectrum range and modulation period, as shown in the Figure below. The spread spectrum settings locate at Page0/0x0E.

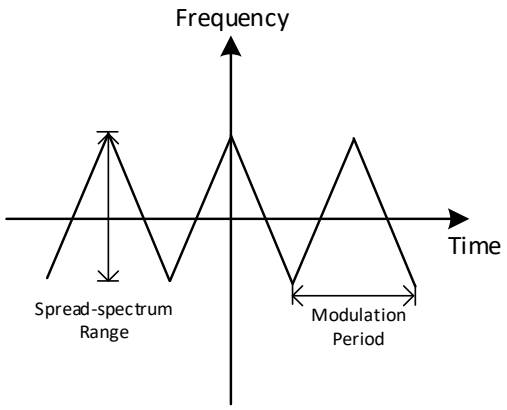


Figure 26 Triangle Spread Spectrum

8.10 I²C Device Address

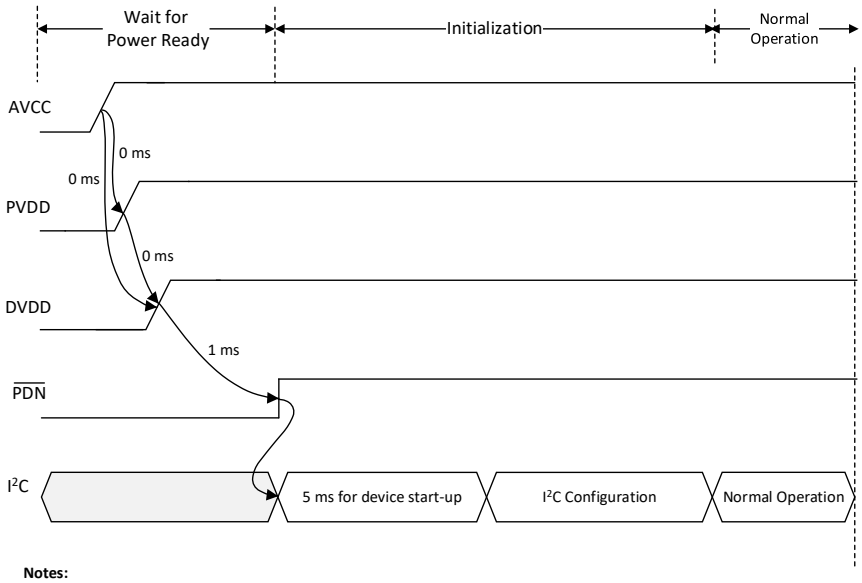
The ACM8816 device has 7 bits for I²C device address. The first five bits (MSBs) of the device address are factory preset to 10000 (0x8x). The next two bits of address byte are the device select bits which can be user-defined by ADR pin in Table 4.

Table 4 I²C Device Address Configuration

ADR PIN Configuration	MSBs					User Define		LSB	Device Write Address
4.7kΩ to DVDD	1	0	0	0	0	0	0	R/W	0x80
15kΩ to DVDD	1	0	0	0	0	0	1	R/W	0x82
47kΩ to DVDD	1	0	0	0	0	1	0	R/W	0x84
120kΩ to DVDD	1	0	0	0	0	1	1	R/W	0x86

8.11 Start-up sequence

1. Configure ADR pin with proper setting for I²C device address.
2. Bring up power supplies (DVDD is needed 1ms before I²C communication).
3. Configure the device via I²C control port based on the user case.
4. The device is now in normal operation.

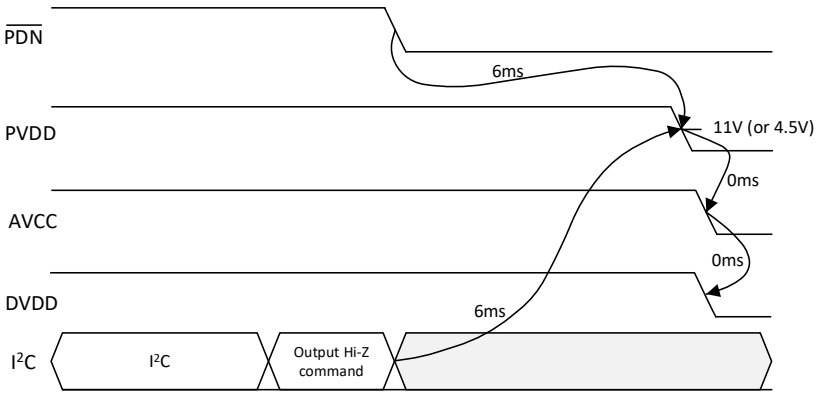


Notes:
- 0ms means no sequence requirement

Figure 27. Start-up Sequence

8.12 Shutdown sequence

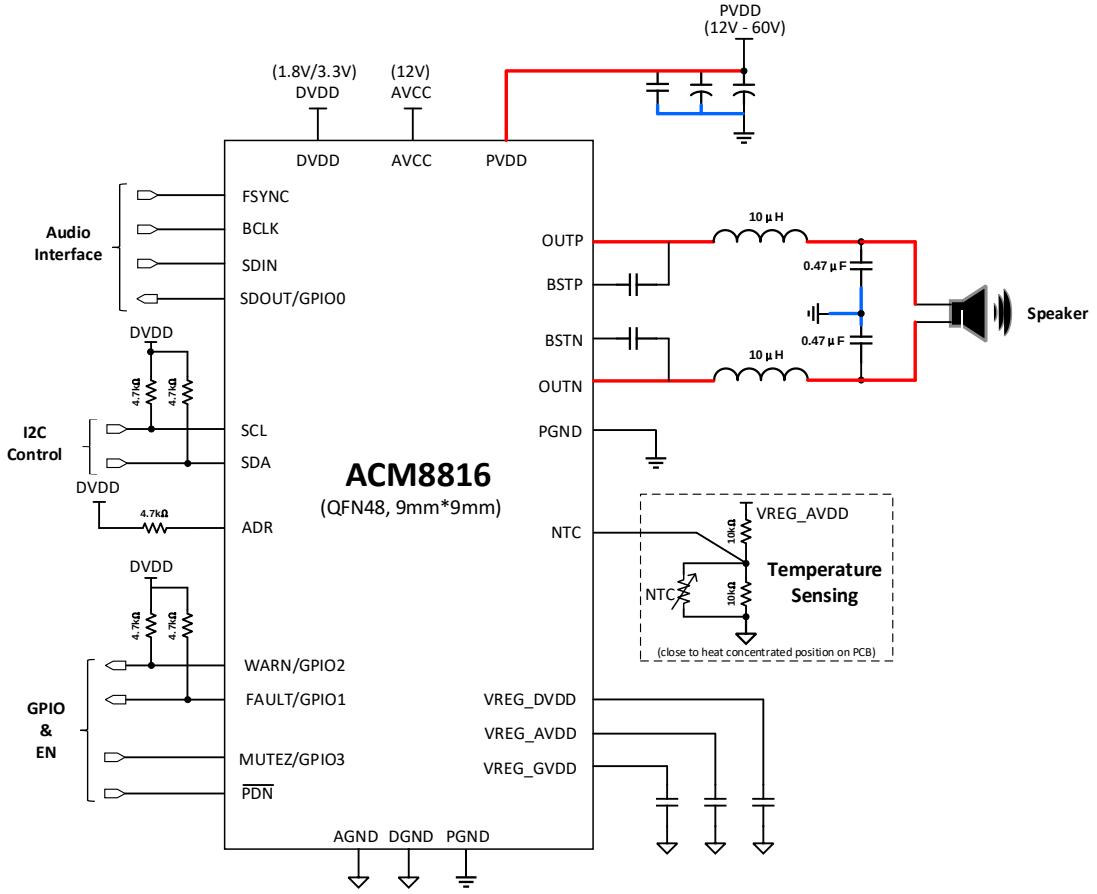
1. The device is in normal operation.
2. Configure the device in digital off state via register 0x04h.
3. Wait at least 6ms (This time depends on the FSYNC rate, digital volume and digital volume ramp down rate).
4. Bring down power supplies.
5. The device is now fully shutdown and powered off.



Notes:
- Before PVDD/DVDD power down, Class D Output driver needs to be disabled by $\overline{PDN}$ or by I²C command.
- At least 6ms delay needed based on LRCLK (F_s) = 48kHz,Digital volume ramp down update every sample period, decreased by 0.5dB for each update, digital volume =24dB.

Figure 28. Shutdown Sequence

9. Application Circuit Example



Note 1: Traces in thick and red/blue should be noticed in PCB layout for high current capability

Note 2: Decoupling capacitors on PVDD should be placed to PVDD pin as close as possible

9 Register Maps

9.1 Control Registers on Page 0

Offset	Acronym	Register Name	Reset Value
0x01	AMP_CTRL1	F_{SW} PWM switching frequency, Fault clear	0x00
0x02	AMP_CTRL2	Analog gain	0x00
0x03	AMP_CTRL3	Loop bandwidth, Undervoltage threshold	0x00
0x04	STATE_CTRL	Reset, Hi-Z / Mute, State Control	0x00
0x05	PROCESSING_CTRL1	AGL, DRB, Hybrid, Post EQ, Sub-CH bypass control	0x12
0x06	PROCESSING_CTRL2	Processing flow selection and power saving selection	0xF0
0x07	I2S_DATA_FORMAT1	I2S data format, length, FSYNC	0x02
0x08	I2S_DATA_FORMAT2	I2S Shift bits	0x00
0x0A	GPIO0_CTRL	GPIO0 enable and function selection. Default function: SDOUT	0x29
0x0B	GPIO1_CTRL	GPIO1 enable and function selection. Default function: WARNZ	0x2B
0x0C	GPIO_FAULT_WARN_SEL1	Fault or Warn masking, including Clipping, OTW, OTSD, Clock Fault, PVDD UV/OV, DC, OC Fault	0xFF
0x0D	GPIO_FAULT_WARN_SEL2	Fault latch/non-latch selection. Fault or Warning masking, including BST UV, AVCC UV/OV, GVDD UV/OV, CBC warning/fault	0x7C
0x0E	SS_CTRL	Spread spectrum setting	0x00
0x0F	VOLUME_CTRL	Volume control	0xCF
0x11	MISC_CTRL	OTSD auto-recovery enable, OTSD auto-recovery delay enable and selection	0x01
0x12	I2S_CLK_FORMAT_RPT1	BCLK ratio (MSB), Sample rate detect	0x00
0x13	I2S_CLK_FORMAT_RPT2	BCLK ratio (LSB)	0x40
0x15	DIEID_RPT	DIE ID	0x16
0x16	STATE_RPT	State report	0x00
0x17	FAULT_RPT1	OTSD, PVDD OV/UV, DC, OC	0x00
0x18	FAULT_RPT2	GVDD_OV, GVDD_UV, CBC_FAULT, CBC_WARN, DC, Clock fault	0x00
0x19	WARN_RPT	Clipping, OTW, external OTW based on NTC	0x00
0x1c	CBC_CTRL0	CBC fault enable	0x88
0x1d	CBC_ CTRL1	CBC window selection, CBC fault/warning enable	0xA4
0x20	MISC_CTRL2	NTC enable, GVDD UV threshold, NTC OTW/OTSD threshold	0x00
0x21	MISC_CTRL3	CBC level	0x00
0x22	LDG_CTRL	OL enable, SL threshold, SL stimulus current,	0x00
0x23	GPIO2_CTRL	GPIO2 enable and function selection. Default function: FAULTZ	0x2B
0x24	GPIO3_CTRL	ClassH GPIO open-drain setting. GPIO3 enable and function selection. Default function: MUTE	0x45

Offset	Acronym	Register Name	Reset Value
0x25	PTSNS_CTRL	GVDD/PVDD voltage sense enable, NTC/internal temperature sensor enable	0x0F
0x26	LDG_CTRL	Load diagnostic setting	0x0F
0x30	LDG_RPT1	Load diagnostic result report 1	0x00
0x31	LDG_RPT2	Load diagnostic result report 2	0x00
0x32	PVDD_SNS_RPT	PVDD voltage sense data report	0x00
0x33	TEMP_SNS_RPT	Temperature sense data report	0x00
0x34	GVDD_SNS_RPT	GVDD voltage sense data report	0x00
0x35	NTC_SNS_RPT	NTC voltage sense data report	0x00
0x7E	XOR_CHECKSUM	XOR Checksum	0x00
0x7F	CRC_CHECKSUM	CRC Checksum	0x00

9.2 Registers Detail Description

9.2.1 Register 1 AMP_CTRL1 (Offset=1h) [Reset=0x00]

7	6	5	4	3	2	1	0
FAULT_CLR	RESERVED			FSW_SEL			RESERVED
R/W	R			R/W			R

Bit	Field	Type	Reset	Description
7	FAULT_CLR	R/W	0	Once write this bit to 1, device will clear analog fault, this bit is auto-clear
6-4	RESERVED	R	000	These bits are reserved
3-1	FSW_SEL	R/W	000	**000: 384kHz** 001: Reserved 010: 480kHz 011: 576kHz 100: 768kHz 101:1024kHz 110: 1536kHz 111: 2048kHz
0	RESERVED	R	0	This bit is reserved

9.2.2 Register 2 AMP_CTRL2 (Offset=2h) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED			ANA_GAIN				
R			R/W				

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	000	These bits are reserved
4-0	ANA_GAIN	R/W	00000	Analog Gain Control, with 0.5dB per step. These bits control the analog gain. **00000: 0dB (67Vp/FS)** 00001: -0.5dB 00010: -1dB … 11111: -15.5dB

9.2.3 Register 3 AMP_CTRL3 (Offset=3h) [Reset=0x00]

7	6	5	4	3	2	1	0
BW_CTRL			BW_CTRL			UV_THRES	
R/W			R/W			R/W	

Bit	Field	Type	Reset	Description
7-5	BW_CTRL	R/W	000	**000: 75kHz** 001: 90kHz 010: 105kHz 011: 125kHz 100: 155kHz 101: 180kHz 110: 220kHz 111: 265kHz
4-1	RESERVED	R/W	000	These bits are reserved
0	UV_THRES	R/W	0	PVDD Undervoltage protection threshold **0: 11V** 1: 4.5V

9.2.4 Register 4 STATE_CTRL (Offset=4h) [Reset=0x00]

7	6	5	4	3	2	1	0
RST_REG	REST_MOD	RESERVED	CH_HIZ	MUTE	CTRL_STATE		
R/W	R/W	R	R/W	R/W	R/W		

Bit	Field	Type	Reset	Description
7	RST_REG	R/W	0	Register Reset **0: Normal** 1: Reset Register
6	RST_MOD	R/W	0	Signal path Reset **0: Normal** 1: Reset Signal path
5, 3	RESERVED	R	00	These bits are reserved
4	CH_HIZ	R/W	0	Force output driver into Hi-Z state **0: Normal State** 1: Change output driver into Hi-Z state
3	MUTE	R/W	0	MUTE Control **0: Normal** 1: Mute
2-0	CTRL_STATE	R/W	000	State Control **000: Digital Off** 001: Analog off 010: Driver Off (Hiz) 011: Play 100: Manual DC LDG

9.2.5 Register 5 PROCESSING_CTRL1 (Offset=5h) [Reset=0x12]

7	6	5	4	3	2	1	0
AGL_BP	DRB_BP	RESERVED		POST_EQ_BP	RESERVED		PROCESSING_BP
R/W	R/W	R		R/W	R		R/W

Bit	Field	Type	Reset	Description
7	AGL_BP	R/W	0	**0: Enable AGL** 1: Bypass AGL
6	DRB_BP	R/W	0	**0: Enable DRB** 1: Bypass DRB
5-4	RESERVED	R	01	These bits are reserved
3	POST_EQ_BP	R/W	0	**0: Enable Post-EQ** 1: Bypass Post-EQ
2-1	RESREVED	R	01	These bits are reserved
0	PROCESSING_BP	R/W	0	**0: Enable audio effect tuning** 1: Bypass all audio effect tuning

9.2.6 Register 6 PROCESSING_CTRL2 (Offset=6h) [Reset=0xF0]

7	6	5	4	3	2	1	0
PROCESS_FLOW_CTRL				POWER_SAVE_DOWN	PLL_CLK_DIV		REAL_96KHZ
R/W				R/W	R/W		R/W

Bit	Field	Type	Reset	Description
7-4	PROCESS_FLOW_CTRL	R/W	1111	Process Flow control Bit [7:6], **11: DRC ON** 00: DRC OFF Bit [5:4], **11: ClassH ON** 00: ClassH OFF
3	POWER_SAVE_DOWN	R/W	0	**0: when have clock fault, device will not shut down analog and digital, only shut down driver** 1: when have clock fault, device will shut down analog and digital and driver
2-1	PLL_CLK_DIV	R/W	00	**00: high PLL frequency** 01: middle PLL frequency 10: low PLL frequency 11: low PLL frequency
0	REAL_96KHZ	R/W	0	**0: 48kHz internal processing** 1: 96kHz internal processing

9.2.7 Register 7 I2S_DATA_FORMAT1 (Offset=7h) [Reset=0x02]

7	6	5	4	3	2	1	0
44K_INPUT	44K_EN	I2S_DATA_FORMATI		I2S_FSYNC_PULSE		I2S_WORD_LENGTH	
R/W	R/W	R/W		R/W		R/W	

Bit	Field	Type	Reset	Description
7	44K_INPUT	R/W	0	**0: 48K/96K input** 1: 44.1K/88.2K input
6	44K_EN	R/W	0	**0: disable 44k input** 1: enable 44k input
5-4	I2S_DATA_FORMAT	R/W	00	**00: I2S** 01: TDM/DSP 10: RTJ 11: LTJ
3-2	I2S_FSYNC_PULSE	R/W	00	**01: FSYNC pulse <8 BCLK. If the high width of LRCLK/FSYNC in TDM/DSP mode is less than 8 cycles of BCLK, these two bits need set to 01.** Others: These bits are reserved
1-0	I2S_WORD_LENGTH	R/W	10	I2S Word length. These bits control both input and output audio interface sample word lengths for DAC operation. 00: 16 bits **01: 20 bits** 10: 24 bits 11: 32 bits

9.2.8 Register 8 I2S_DATA_FORMAT2 (Offset=8h) [Reset=0x00]

7	6	5	4	3	2	1	0
I2S_LEFT_BITS_SHIFT							
R/W							

Bit	Field	Type	Reset	Description
7-0	I2S_LEFT_BIT_SHIFT	R/W	00000000	Control the offset of Left Channel audio data in the audio frame for both input and output. The offset is defined as the number of BLCK from the starting (MSB) of audio frame to the starting of the desired audio sample. **00000000: offset = 0 BCLK (no offset)** 00000001: offset = 1 BCLK …….. 11111111: offset = 256 BCLK

9.2.9 Register 9 GPIO0_CTRL (Offset=0Ah) [Reset=0x29]

7	6	5	4	3	2	1	0
RESERVED		GPIO0_OE	GPIO0_FUNC_SEL				
R		R/W	R/W				

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00	These bits are reserved
5	GPIO0_OE	R/W	1	0: GPIO0 is input **1: GPIO0 is output**
4-0	GPIO0_FUNC_SEL	R/W	01001	00000: off(low) 00001: digital off 00010: analog off 00011: driver off 00100: mute 00110: clock invalid flag(clock error or clock missing) 00111: pll lock flag 01000: GPIO0 as WARNZ output **01001: serial audio interface data output (SDOUT)** 01011: GPIO0 as FAULTZ output 01100: resetz 01111: Class H Control Signal Output

9.2.10 Register 10 GPIO1_CTRL (Offset=0Bh) [Reset=0x2B]

7	6	5	4	3	2	1	0
RESERVED		GPIO1_OE	GPIO1_FUNC_SEL				
R		R/W	R/W				

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00	These bits are reserved
5	GPIO1_OE	R/W	1	0: GPIO1 is input **1: GPIO1 is output**
4-0	GPIO1_FUNC_SEL	R/W	01011	DEFAULT is FAULT pin 00000: off(low) 00001: digital off 00010: analog off 00011: driver off 00100: mute 00110: clock invalid flag(clock error or clock missing) 00111: pll lock flag 01000: GPIO1 as WARNZ output 01001: serial audio interface data output (SDOUT)

Bit	Field	Type	Reset	Description
				01011: GPIO1 as FAULTZ output (default) 01100: resetz 01111: Class H Control Signal Output

9.2.11 Register 11 GPIO_FAULT_WARN_SEL1 (Offset=0Ch) [Reset=0xFF]

7	6	5	4	3	2	1	0
CLIP	OTW	OTSD	CLK_FAULT	PVDD_UV	PVDD_OV	DC	OC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	CLIP	R/W	1	CLIP warning report 0: Mask; **1: Report**
6	OTW	R/W	1	Global over temperature warning report 0: Mask; **1: Report**
5	OTSD	R/W	1	Global over temperature shutdown fault report 0: Mask; **1: Report**
4	CLK_FAULT	R/W	1	Clock fault report 0: Mask; **1: Report**
3	PVDD_UV	R/W	1	PVDD undervoltage fault report 0: Mask; **1: Report**
2	PVDD_OV	R/W	1	PVDD overvoltage fault report 0: Mask; **1: Report**
1	DC	R/W	1	DC output fault report 0: Mask; **1: Report**
0	OC	R/W	1	Over current fault report 0: Mask; **1: Report**

9.2.12 Register 12 GPIO_FAULT_WARN_SEL2(Offset=0Dh) [Reset=0x7C]

7	6	5	4	3	2	1	0
FAULT_LATCH	BST_UV	AVCC_OV	AVCC_UV	GVDD_UV	GVDD_OV	CBC_FAULT	CBC_WARN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7	FAULT_LATCH	R/W	0	Select fault pin latch behavior **0: Latch;** 1: Non-Latch
6	BST_UV	R/W	1	Bootstrap Undervoltage protection 0: Mask; **1: Report**
5	AVCC_OV	R/W	1	AVCC overvoltage fault 0: Mask; **1: Report**
4	AVCC_UV	R/W	1	AVCC undervoltage fault

Bit	Field	Type	Reset	Description
				0: Mask; **1: Report**
3	GVDD_OV	R/W	1	GVDD overvoltage fault 0: Mask; **1: Report**
2	GVDD_UV	R/W	1	GVDD undervoltage fault 0: Mask; **1: Report**
1	CBC_FAULT	R/W	1	Cycle-by-cycle current limit fault 0: Mask; **1: Report**
0	CBC_WARN	R/W	1	Cycle-by-cycle current limit warning 0: Mask; **1: Report**

9.2.13 Register 13 SS_CTRL (Offset=0Eh) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED	SS_FORCE_DUTY	SS_EXPEND_STEP_CYCLES		RESERVED		RDM_EN	TRI_EN
R	R/W	R/W		R		R/W	R/W

Bit	Field	Type	Reset	Description
7	RESERVED	R	0	This bit is reserved
6	SS_FORCE_DUTY	R/W	0	Set this bit is required to be set to 1 when Spread spectrum is enabled
5:4	SS_EXPEND_STEP_CYCLES	R/W	00	Set the triangle spread spectrum modulation frequency dividing factor **00: 1×SS frequency (default)** 01: 1/2×SS frequency 10: 1/3×SS frequency 11: 1/4×SS frequency
3:2	RESERVED	R	00	These bits are reserved
1	RDM_EN	R/W	0	**0: Random SS disable (default)** 1: Random SS enable
0	TRI_EN	R/W	0	**0: Triangle SS disable (default)** 1: Triangle SS enable

9.2.14 Register 14 VOLUME_CTRL (Offset=0Fh) [Reset=0xCF]

7	6	5	4		3	2	1	0
VOL								
R/W								

Bit	Field	Type	Reset	Description
7-0	VOL	R/W	11001111	Volume control. 00000000: -104dB 11010000: 0dB 11010001: 0.5dB

Bit	Field	Type	Reset	Description
				…. 11111111: 24dB

9.2.15 Register 15 MISC_CTRL (Offset=11h) [Reset=0x01]

7	6	5	4	3	2	1	0
RESERVED				LPD_MODULATION	OTSD_AUTO_REC	OTSD_REC_DLY	OTSD_REC_DLY_EN
R				R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000	These bits are reserved
3	LPD_MODULATION	R/W	0	Modulation selection **0: High performance modulation** 1: Low power dissipation Modulation
2	OTSD_AUTO_REC	R/W	0	Auto recover enable/disable from OTSD fault **0: OT auto-recovery disable** 1: OT auto-recovery enable
1	OTSD_REC_DLY	R/W	0	Delay time selection for OTSD fault auto recovery **0: 1ms** 1: 1s
0	OTSD_REC_DLY_EN	R/W	1	Enable or disable the delay for OTSD fault auto recovery 0: Delay disable **1: Delay enable**

9.2.16 Register 16 I2S_CLK_FORMAT_RPT1 (Offset=12h) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED		BCLK_RATIO_HIGH		FS_DET			
R		R		R			

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00	These bits are reserved
5-4	BCLK_RATIO_HIGH	R	00	These bits indicate the BCLK ratio, the number of BCLK in one audio frame. BCLK=32FS-512FS MSB Bit [9-8].
3-0	FS_DET	R	0000	These bits indicate the currently detected audio sample rate. 0110: 32kHZ 1000: 44.1kHZ 1001: 48kHZ 1010: 88.2kHZ 1011: 96kHZ 1101: 192kHz

9.2.17 Register 17 I2S_CLK_FORMAT_RPT2 (Offset=13h) [Reset=0x40]

7	6	5	4	3	2	1	0
BCLK_RATIO_LOW							
R							

Bit	Field	Type	Reset	Description
7-0	BCLK_RATIO_LOW	R	01000000	These bits indicate the BCLK ratio, the number of BCLK in one audio frame. LSB Bit [7-0].

9.2.18 Register 18 DIEID_RPT (Offset=15h) [Reset=0x16]

7	6	5	4	3	2	1	0
DIEID_RPT							
R							

Bit	Field	Type	Reset	Description
7-0	DIE_ID	R	00010110	DIE ID

9.2.19 Register 19 STATE_RPT (Offset=16h) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED						STATE_RPT	
R						*R*	

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000	These bits are reserved
1-0	STATE_RPT	R	00	**00: Digital Off (default)** 01: Analog Off 10: Driver Off (Hiz) 11: Play

9.2.20 Register 20 FAULT_RPT1(Offset=17h) [Reset=0x00]

7	6	5	4	3	2	1	0
OTSD_NTC	OTSD	PVDD_OV	PVDD_UV	AVCC_OV	AVCC_UV	BST_UV	OC
R	R	R	R	R	R	R	R

Bit	Field	Type	Reset	Description
7	OTSD_NTC	R	0	Over temperature shutdown fault report based on external NTC **0: Normal**

Bit	Field	Type	Reset	Description
				1: NTC Over temperature shutdown fault
6	OTSD	R	0	Over temperature shutdown fault report **0: Normal** 1: Over temperature shutdown fault report
5	PVDD_OV	R	0	PVDD overvoltage fault report **0: Normal** 1: PVDD over-voltage fault
4	PVDD_UV	R	0	PVDD undervoltage fault **0: Normal** 1: PVDD under-voltage fault report
3	AVCC_OV	R	0	AVCC overvoltage fault **0: Normal** 1: AVCC overvoltage fault report
2	AVCC_UV	R	0	AVCC undervoltage fault **0: Normal** 1: AVCC undervoltage fault report
1	BST_UV	R	0	BST undervoltage fault **0: Normal** 1: BST undervoltage fault report
0	OC	R	0	Over current fault **0: Normal** 1: Over current fault report

9.2.21 Register 21 FAULT_RPT2(Offset=18h) [Reset=0x00]

7	6	5	4	3	2	1	0
GVDD_OV	GVDD_UV	CBC_FAULT	CBC_WARN	DC	CLK_FAULT	RESERVED	
R	R	R	R	R	R	R	

Bit	Field	Type	Reset	Description
7	GVDD_OV	R	0	GVDD overvoltage fault report **0: Normal** 1: GVDD overvoltage fault
6	GVDD_UV	R	0	GVDD undervoltage fault report **0: Normal** 1: GVDD undervoltage fault
5	CBC_FAULT	R	0	Cycle-by-cycle current limit fault report **0: Normal** 1: Cycle-by-cycle current limit fault
4	CBC_WARN	R	0	Cycle-by-cycle current limit warning report **0: Normal** 1: Cycle-by-cycle current limit warning

Bit	Field	Type	Reset	Description
3	DC	R	0	DC output fault report **0: Normal** 1: DC output fault
2	CLK_FAULT	R	0	Clock fault report **0: Normal** 1: Clock fault
1-0	RESERVED	R	00	These bits are reserved

9.2.22 Register 22 WARN_RPT(Offset=19h) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED					CLIP	OTW_NTC	OTW
R					R	R	R

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	000000	These bits are reserved
2	CLIP	R	0	Clip warning report **0: Normal** 1: Clipp warning
1	OTW_NTC	R	0	Over temperature warning report based on external NTC **0: Normal** 1: Over temperature warning(NTC)
0	OTW	R	0	Over temperature warning report **0: Normal** 1: Over temperature warning

9.2.23 Register 23 CBC_CTRL0(Offset=1Ch) [Reset=0x88]

7	6	5	4	3	2	1	0
CBC_FAULT_DIS	RESERVED						
R/W	R						

Bit	Field	Type	Reset	Description
7	CBC_FAULT_DIS	R/W	1	CBC Fault sequence enable/disable. If enabled, the device stops switching when CBC fault happens. 0: Stop switching when CBC Fault happens **1: Keep switching when CBC Fault happens**
6:0	RESERVED	R	001000	These bits are reserved.

9.2.24 Register 24 CBC_CTRL1(Offset=1Dh) [Reset=0xA4]

7	6	5	4	3	2	1	0
RESERVED						CBC_FAULT_EN	CBC_WARN_EN

R	R/W	R/W

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	101001	These bits are reserved.
1	CBC_FAULT_EN	R/W	0	CBC Fault control **0: Disable CBC feature and Fault report** 1: Enable CBC feature and Fault report
0	CBC_WARN_EN	R/W	0	CBC Warning control **0: Disable CBC feature and Warning report** 1: Enable CBC feature and Warning report

9.2.25 Register 25 MISC_CTRL2 (Offset=20h) [Reset=0x00]

7	6	5	4	3	2	1	0
NTC_OT_DIS	GVDD_UV_SEL	NTC_OTW_SEL	OTW_SEL		OTSD_SEL		RESERVED
R/W	R/W	R/W	R/W		R/W		R

Bit	Field	Type	Reset	Description
7	NTC_OT_DIS	R/W	0	NTC over temperature protection enable/disable report **0: Enable NTC over temperature protection report** 1: Disable NTC over temperature protection report
6	GVDD_UV_SEL	R/W	0	GVDD undervoltage protection threshold **0: 3.6V** 1: 3V
5	NTC_OTW_SEL	R/W	0	NTC over temperature warning protection threshold **0: 1.2V** 1: 1.1V
4:3	OTW_SEL	R/W	00	Over temperature warning threshold **00: 95℃** 01: 105℃ 10: 125℃ 11: 135℃
2:1	OTSD_SEL	R/W	00	Over temperature shutdown threshold **00: 135℃** 01: 145℃ 10: 155℃ 11: 160℃
0	RESERVED	R	0	This bit is reserved

9.2.26 Register 26 MISC_CTRL3 (Offset=21h) [Reset=0x00]

7	6	5	4	3	2	1	0
CBC_LEVEL			RESERVED				
R/W			R				

Bit	Field	Type	Reset	Description
7:5	CBC_LEVEL	R/W	000	Cycle-by-cycle current limit threshold **000: 70%** 001: 80% 010: 90% 011: Reserved 100: Reserved 101: 40% 110: 50% 111: 60%
4:0	RESERVED	R	00000	These bits are reserved

9.2.27 Register 27 LDG_CTRL (Offset=22h) [Reset=0x00]

7	6	5	4	3	2	1	0
LDG_OL_SEL	LDG_SL_SEL		RESERVED				
			R				

Bit	Field	Type	Reset	Description
7	LDG_OL_SEL	R/W	0	Open Load detection threshold select for DC load diagnostics **0: 45Ω** 1: 70Ω
6:5	LDG_SL_SEL	R/W	00	Short Load detection threshold select for DC load diagnostics **00: 0.5Ω** 01: 0.7Ω 10: 0.8Ω 11: 1.0Ω
4:0	RESERVED	R	00000	These bits are reserved

9.2.28 Register 28 GPIO2_CTRL (Offset=23h) [Reset=0x2B]

7	6	5	4	3	2	1	0
RESERVED		GPIO2_OE	GPIO2_FUNC_SEL				
R		R/W	R/W				

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00	These bits are reserved
5	GPIO2_OE	R/W	1	0: GPIO2 is input **1: GPIO2 is output**
4-0	GPIO2_FUNC_SEL	R/W	01011	00000: off(low) 00001: digital off 00010: analog off 00011: driver off

Bit	Field	Type	Reset	Description
				00100: mute 00110: clock invalid flag(clock error or clock missing) 00111: pll lock flag 01000: GPIO2 as WARNZ output 01001: serial audio interface data output (SDOUT) **01011: GPIO2 as FAULTZ output** 01100: resetz 01111: Class H Control Signal Output

9.2.29 Register 29 GPIO3_CTRL (Offset=24h) [Reset=0x45]

7	6	5	4	3	2	1	0
RESERVED	GPIO_CLASSH_OD	GPIO3_OE	GPIO3_FUNC_SEL				
R	R/W	R/W	R/W				

Bit	Field	Type	Reset	Description
7	RESERVED	R	00	These bits are reserved
6	GPIO_CLASSH_OD	R/W	1	Set ClassH GPIO open-drain 0: GPIO is push-pull **1: GPIO is open-drain**
5	GPIO3_OE	R/W	0	0: GPIO3 is input 1: GPIO3 is output
4-0	GPIO3_FUNC_SEL	R/W	00101	00000: off(low) 00001: digital off 00010: analog off 00011: driver off **00101: mute** 00110: clock invalid flag(clock error or clock missing) 00111: pll lock flag 01000: GPIO3 as WARNZ output 01001: serial audio interface data output (SDOUT) 01011: GPIO3 as FAULTZ output 01100: resetz 01111: Class H Control Signal Output

9.2.30 Register 30 PTSNS_CTRL(Offset=25h) [Reset=0x0F]

7	6	5	4	3	2	1	0
RESERVED				GVDD_SNS_EN	NTC_SNS_EN	TEMP_SNS_EN	PVDD_SNS_EN
R				R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000	These bits are reserved.
3	GVDD_SNS_EN	R/W	1	GVDD voltage sense enable 0: disable **1: enable**
2	NTC_SNS_EN	R/W	1	NTC temperature sense enable 0: disable **1: enable**
1	TEMP_SNS_EN	R/W	1	Internal temperature sense enable 0: disable **1: enable**
0	PVDD_SNS_EN	R/W	1	PVDD voltage sense enable 0: disable **1: enable**

9.2.31 Register 31 LDG_CTRL(Offset=26h) [Reset=0x0F]

7	6	5	4	3	2	1	0
RESERVED				SLOL_EN	S2G_EN	S2P_EN	LDG_ABORT
R				R/W	R/W	R/W	R/W

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000	These bits are reserved.
3	SLOL_EN	R/W	1	DC Load diagnostic, Short Load and Open 0: disable **1: enable**
2	S2G_EN	R/W	1	DC Load diagnostic, Short to GND 0: disable **1: enable**
1	S2P_EN	R/W	1	DC Load diagnostic, Short to PVDD 0: disable **1: enable**
0	LDG_ABORT	R/W	1	Abort current DC Load diagnostic 0: normal **1: abort**

9.2.32 Register 32 LDG_RPT1(Offset=30h) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED			DC_LDG_DONE	SL_FAULT	OL_FAULT	S2G_FAULT	S2P_FAULT
R			R	R	R	R	R

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	000	These bits are reserved.
4	DC_LDG_DONE	R	0	This bit will be set to 1 once the DC load diagnostic is completed
3	SL_FAULT	R	0	DC Load diagnostic, Short Load detection result 0: normal load **1: Short load fault detected**
2	OL_FAULT	R	0	DC Load diagnostic, Open Load detection result 0: normal load **1: Open load fault detected**
1	S2G_FAULT	R	0	DC Load diagnostic, Short to GND detection result 0: disable **1: Short to GND fault detected**
0	S2P_FAULT	R	0	Abort current DC Load diagnostic 0: disable **1: Short to PVDD fault detected**

9.2.33 Register 33 LDG_RPT2(Offset=31h) [Reset=0x00]

7	6	5	4	3	2	1	0
RESERVED				S2PP_FAULT	S2PN_FAULT	S2GP_FAULT	S2GN_FAULT
R				R	R	R	R

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	000	These bits are reserved.
3	S2PP_FAULT	R	0	OUTP Short to power detection result 0: normal load **1: Short to PVDD fault detected**
2	S2PN_FAULT	R	0	OUTN Short to power detection result 0: normal load **1: Short to PVDD fault detected**
1	S2GP_FAULT	R	0	OUTP Short to GND detection result 0: disable **1: Short to GND fault detected**
0	S2GN_FAULT	R	0	OUTN Short to GND detection result 0: disable **1: Short to GND fault detected**

9.2.34 Register 34 PVDD_SNS_RPT(Offset=32h) [Reset=0x00]

7	6	5	4	3	2	1	0
PVDD_SNS_RPT							
R							

Bit	Field	Type	Reset	Description
7:0	PVDD_SNS_RPT	R	00000000	PVDD voltage sense result PVDD = 85*code (in dec) /255

9.2.35 Register 35 TEMP_SNS_RPT(Offset=33h) [Reset=0x00]

7	6	5	4	3	2	1	0
TEMP_SNS_RPT							
R							

Bit	Field	Type	Reset	Description
7:0	TEMP_SNS_RPT	R	00000000	Temperature sense result. Temperature = -57 + code (in dec)

9.2.36 Register 36 GVDD_SNS_RPT(Offset=34h) [Reset=0x00]

7	6	5	4	3	2	1	0
GVDD_SNS_RPT							
R							

Bit	Field	Type	Reset	Description
7:0	GVDD_SNS_RPT	R	00000000	GVDD voltage sense result GVDD voltage = 8 * code(in dec)/255

9.2.37 Register 37 NTC_SNS_RPT(Offset=35h) [Reset=0x00]

7	6	5	4	3	2	1	0
NTC_SNS_RPT							
R							

Bit	Field	Type	Reset	Description
7:0	NTC_SNS_RPT	R	00000000	NTC voltage sense result NTC voltage = 2.5 * code (in dec)/255

9.2.38 Register 38 XOR_CHECKSUM(Offset=7Eh) [Reset=0x00]

7	6	5	4	3	2	1	0
XOR_CHECKSUM							
R							

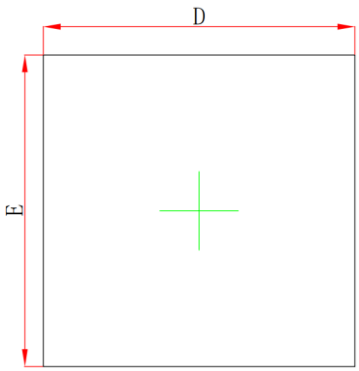
Bit	Field	Type	Reset	Description
7-0	XOR_CHECKSUM	R	00000000	XOR checksum result

9.2.39 Register 39 CRC_CHECKSUM(Offset=7Fh) [Reset=0x00]

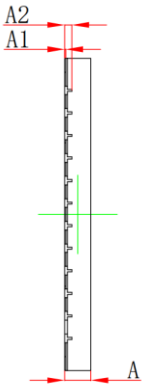
7	6	5	4	3	2	1	0
CRC_CHECKSUM							
R							

Bit	Field	Type	Reset	Description
7-0	CRC_CHECKSUM	R	00000000	CRC checksum result

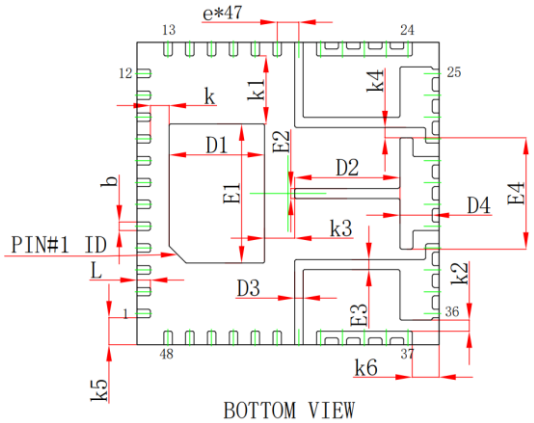
10. Package Dimensions



TOP VIEW
[正视图]



SIDE VIEW
[侧视图]



BOTTOM VIEW
[背视图]

		SYMBOL	MIN.	NOM.	MAX.
TOTAL THICKNESS		A	0.700	0.750	0.800
STAND OFF		A1	0	--	0.050
L/F THICKNESS		A2		0.203REF.	
LEAD WIDTH		b	0.200	0.250	0.300
BODY SIZE	X	D		9.000BSC.	
	Y	E		9.000BSC.	
LEAD PITCH		e		0.650BSC.	
EP SIZE	X	D1	2.740	2.840	2.940
	Y	E1	4.040	4.140	4.240
	X	D2	3.035	3.135	3.235
	Y	E2	0.200	0.300	0.400
	X	D3	0.150	0.250	0.350
	Y	E3	0.200	0.300	0.400
	X	D4	0.865	0.965	1.065
	Y	E4	3.220	3.320	3.420
LEAD LENGTH		L	0.350	0.400	0.450
LEAD TIP TO EP EDGE		k		0.560REF.	
		k1		2.030REF.	
		k2		0.330REF.	
EP EDGE TO EP EDGE		k3		0.900REF.	
		k4		0.305REF.	
LEAD EDGE TO PKG EDGE		k5		0.800REF.	
		k6		0.800REF.	

11. Ordering Information

Orderable Device	Package Type	MPQ	MOQ	Eco Plan	MSL Level	Device Marking
ACM8816	QFN 48 Tape and Reel	1000	1000	RoHS Compliant Lead-Free Finish	MSL3	ACM8816

12. Revise History